

Seat No.:	Q. Paper Code: FTC-A-003			SET	A		
	Fabtech Technical Campus, College of Engineering & Research, Sangola						
	(An Autonomous Institute)						
	Electronics and Telecommunication Engineering						
	Academic Year: -2025-26, Semester-I						
CMOS VLSI Design (25PET11171)							
Regular End Semester Examination Winter 2025-26 [Dec/Jan]							
Class:	F. Y. M. Tech.	Day & Date:	Thursday, 01/01/2026				
Duration:	03 Hrs.	Max. Marks:	60 Marks				
Time:	11:00 AM TO 02:00 PM						
Instructions:							
1) All Questions are compulsory. 2) Figures to the right indicate full marks. 3) Draw neat diagram wherever necessary. 4) Make suitable assumptions if necessary and state it clearly. 5) Use of non-programmable calculator is allowed.							
Q. No.	Questions				Marks	CO	BL
Q. 1	Attempt any two of the following				12		
1	Summarize the properties of static CMOS inverter?.				6	1	4
2	Explain in detail about power consumption in CMOS Inverter.				6	1	3
3	Explain about DC characteristics of the CMOS inverter.				6	1	2
Q. 2	Attempt any two of the following				12		
1	What is pseudo nMOS?				6	2	2
2	Apply NMOS logic and draw the logic diagram of two input NOR gate and NAND gate.				6	2	3
3	What is Pass transistor logic? Outline the advantages of pass transistor logic.				6	2	1
Q. 3	Attempt any two of the following				12		
1	List out the timing parameters of a Flip-flop.				6	3	1
2	What is Pass transistor logic? Outline the advantages of pass transistor logic				6	3	2
3	Compare Static and Dynamic sequential circuits.				6	3	4
Q. 4	Attempt any two of the following				12		

1	Design a 4-bit Ripple Carry Adder and explain the propagation of carry signals.	6	4	6
2	Explain the architecture of an array multiplier and discuss its advantages and disadvantages.	6	4	4
3	Explain the SRAM cell structure and compare it with DRAM in terms of speed, area, and power.	6	4	4
Q. 5	Attempt any two of the following	12		
1	What is Verilog HDL? Explain its role in modern digital system design.	6	5	2
2	Explain gate-level modeling with a Verilog example.	6	5	3
3	Design 4:1 Multiplexer using a) If-else statement b) Case statement	6	5	6